CLAIMS

1. A digital system for receiving an input digital signal and for generating an output digital signal that is related to the input digital signal comprising:

a) a signal level booster having an input configured to be in communication with a signal that is reflective of the input digital signal and an output that is reflective of the input to said signal level booster, but of greater magnitude;

b) a first latch having an input in communication with the output of said signal level booster, configured to be toggled by the output of said signal level booster and by a first clock signal, and having an output;

c) digital logic having an input in communication with a signal that is reflective of the output of said first latch and having an output; and

d) a second latch having an input in communication with the output of said digital logic, configured to be toggled by the output of said digital logic and by the first clock signal, and having an output configured to deliver the output digital signal.

2. The digital system of claim 1 in which a jam latch functions as said signal level booster and said first latch.

3. The digital system of claim 2 in which said second latch includes an n-latch.

4. The digital system of claim 1 in which said second latch includes an n-latch.

5. The digital system of claim 1 in which the input digital signal and the output digital signal are each a single signal.

6. The digital system of claim 1 in which the input digital signal and the output digital signal are each a complementary pair of signals.

7. The digital system of claim 1 further including a clocked buffer configured to be powered by a second clock signal that is complementary to and substantially non-overlapping with the first clock signal and having an input configured to be in communication with the input digital signal and having an output in communication with said signal level booster.

8. The digital system of claim 7 in which the second clock signal is an adiabatic signal.

9. The digital system of claim 8 in which the adiabatic signal includes blips.

10. The digital system of claim 8 in which the adiabatic signal includes a staircase signal.

11. The digital system of claim 8 in which the adiabatic signal includes a ramp signal.

12. The digital system of claim 8 in which the input digital signal is a complementary pair of signals and in which the input to said clocked buffer is configured to be in communication with the complementary pair of signals.

13. The digital system of claim 8 further including a third latch having an input in communication with the output of said first latch, configured to be toggled by the output of said first latch and by the second clock signal, and having an output in communication with the input to said digital logic.

14. The digital system of claim 13 in which said third latch includes an n-latch.

15. The digital system of claim 14 in which said jam latch functions as said signal level booster and said first latch.

16. The digital system of claim 15 in which said second latch includes an n-latch.

17. A method for generating an output digital signal that is related to an input digital signal comprising:

a) boosting an incoming signal that is reflective of the input digital signal;

b) latching the boosted signal under the control of a first clock signal;

c) processing a pre-processed signal that is reflective of the latched signal with digital logic;

d) latching the processed signal under the control of the first clock; and

e) delivering the latched processed signal as the output digital signal.

18. The method of claim 17 in which the input digital signal and the output digital signal are each a single signal.

19. The method of claim 17 in which the input digital signal and the output digital signal are each a complementary pair of signals.

20. The method of claim 17 further including clocking the input digital signal under the power of a second clock signal that is complementary to and substantially non-overlapping with the first clock signal and delivering this clocked signal as the incoming signal.

21. The method of claim 20 in which the second clock signal is an adiabatic signal.

22. The method of claim 21 in which the adiabatic signal includes blips.

23. The method of claim 21 in which the adiabatic signal includes a staircase signal.

24. The method of claim 21 in which the adiabatic signal includes a ramp signal.

25. The method of claim 21 in which the input digital signal is a complementary pair of signals and in which the clocked signal is based on the complementary pair of signals.

26. The method of claim 21 further including latching the latched signal under the control of the second clock signal and delivering that twice latched signal as the pre-processed signal.

27. A digital system comprising:

a) a clocked buffer;

b) a signal line having two ends, one end of which is in communication with said clocked buffer;

c) a jam latch in communication with the other end of said signal line;

d) digital logic in communication with said jam latch; and

e) a first n-latch in communication with said digital logic.

28. The digital system of claim 27 further including a second n-latch in communication with said jam latch and said digital logic.

29. The digital system of claim 28 wherein:

a) said jam latch and said first n-latch are controlled by a first clock signal; and

b) said clocked buffer and said second n-latch are controlled by a second clock signal that is complementary to and substantially non-overlapping with the first clock signal.

30. A clock-powered logic system containing logic configured to be connected to a supply voltage and configured to be powered by at least one clock having a voltage of a magnitude that does not exceed the magnitude of the supply voltage.

31. The clock-powered logic system of claim 30 in which said logic is configured to be powered by at least one clock having a voltage of a magnitude that is less than the magnitude of the supply voltage.

32. The clock-powered logic system of claim 30 in which said system includes a jam latch.

33. The clock-powered logic system of claim 30 in which said system includes a level booster circuit.

34. The clock-powered logic system of claim 30 in which said system includes a pulse-to- level converter.

35. The clock-powered logic system of claim 30 in which said system includes an n-latch.

36. The clock-powered logic system of claim 30 in which said system includes a device that can be clocked by a signal of smaller magnitude than the supply voltage.

37. The clock-powered logic system of claim 30 in which said system includes a clocked buffer.

38. The clock-powered logic system of claim 30 in which said system is configured to utilize an adiabatic signal.

39. The clock-powered logic system of claim 38 in which the adiabatic signal includes blips.

40. The clock-powered logic system of claim 38 in which the adiabatic signal includes a staircase signal.

41. The clock-powered logic system of claim 38 in which the adiabatic signal includes a ramp signal.